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# A Full Adder Cell Based on MOSFET Technology to Apply in Arithmetic Circuits

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**Abstract**

*In this paper, a full adder cell based on a parallel design using MOSFET technology is presented. The main goal of designing this full adder cell is to reduce critical path delay in adder circuits. The proposed design by reduces length of data path and positively, affects speed and power consumption parameters. In order to evaluate the proposed full adder cell, several simulations are performed in different load capacitors, frequencies and temperatures using HSPICE in 32nm CMOS technologies. The proposed full adder cells were compared with ten other full adder cells using 4-bit Ripple Carry Adder (RCA) and 8-bit RCA circuits in power consumption, speed, and Power Delay Product (PDP) parameters. The obtained results indicate that the proposed design is faster than other designs due to a shortened data path. The results of the simulations confirm the higher efficiency of the proposed full adder cell with respect to other designs.*

***Keywords:*** *arithmetic circuits, Critical path delay, Full adder cell, speed.*

## 1. Introduction

In digital computers, arithmetic circuits take over the main activities in data processing. These circuits created the required results for solving mathematical arithmetic problems by receiving and processing the data. Other arithmetic operations can adjust by four main arithmetic operations and scientific problems may be solved by using numerical calculation methods. In RISCs, it is intended to reduce arithmetic instructions and as a result, integrate fewer arithmetic circuits. The other instructions are calculated using numerical calculation methods by the existing circuits. Meanwhile, addition is among one of the main arithmetic circuits and the other arithmetic circuits can be calculated by using addition operation. In many systems, the adders determine the overall efficiency of the system. All these cases can be important reasons for designing and improving adder circuits [1]-[5].

The structure of the full adder cell directly affects the efficiency of adder circuits. Full adder cell is a circuit having three inputs and two outputs. The outputs are equal to the addition of the inputs. The RCA circuit is formed for adding two n-bit numbers such as A and B that consists of n full adder cells. Ai and Bi are the ith bit of the two numbers A and B, and carry input (Cin) that derives from the previous full adder, enters as the inputs of ith full adder cell. Sum output and carry output (Cout) is the addition

result of these three inputs. The equations related to the outputs of a full adder cell can be defined as equations (1) and (2) [6].

$$\mathrm{Sum} = A_i \oplus B_i \oplus C_{in} \quad (1)$$

$$\mathrm{Cout} = A_i B_i + A_i C_{in} + B_i C_{in} \quad (2)$$

RCAs have less hardware overhead than parallel adders. But, the main defect of RCAs is their high delay because the data path is too lengthy. Hence, finding solutions to shorten the delay of data path in these adders is deemed of value [7]. Achieving this goal is the main reason of presenting a new full adder cell based on a parallel structure in this paper. In n-bit RCA, the delay of data path is equal to the summation of delay of the containing full adder cells that is delay in n full adder cells. But using the proposed full adder cells in n-bit RCA circuit, the delay in its data path is equal to the summation of delay of one adder cell and (n-1) multiplexer 2 to 1. In proposed design, multiplexers are used so that the delay is equal to one transistor. Consequently, RCA delay will be equal to the summation of delays of one full adder cell and (n-1) transistors [8], [9]. The simulation results of implemented adder using the proposed full adder cell confirm this point.

The rest of this paper is organized as follows: previous works is reviewed in section 2. In section 3, the proposed full adder cell will be presented. Simulation results and comparison of the proposed design with other design are provided in section 4. Finally, conclusion is given in section 5.

## 2. Previous Works

Several methods have been presented for designing a full adder cell because of the significant of full adder cell efficiency. Others are faster and the other ones have lower power consumption. Hence, Power Delay Product (PDP) parameter is used and compares them so that a tradeoff between delay and power consumption parameters of the circuit. In this section some new full adders are selected in CMOS technologies.

The first full adder cell that is studied is the CMOS-Bridge cell which uses a bridge technique for output production [10]. The circuit of this cell is made up of 24 transistors that is shown in Figure1. First created complement of Cout output with the use of a bridge network,. The output of this function enters a network bridge and an inverter gate to create Cout and Sum outputs respectively. One of the advantages of this design is its structure that simply leads to circuit layout. But the main defect of this design is its lengthy path leading to high delay.

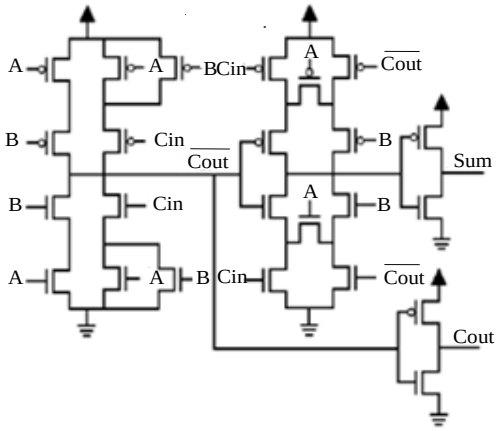


***Figure 1. CMOS-Bridge Full Adder Cell Presented in [10]***

The second design is a full adder cell that we will reveal it to be TG-CMOS and present in [11]. Its circuit is based on transmission gates and shown in Figure2. This design, benefits from the advantages of transmission gate. Contrary to Pass Transistor, transmission gate has full swing outputs. In other words, unlike Pass transistors, transmission gate does not involve with the problem of losing threshold voltage. The defect of transmission gate compared to Pass Transistor logic is that it makes use of more transistors. This model is composed of 20 transistors and its critical path includes four transistors.

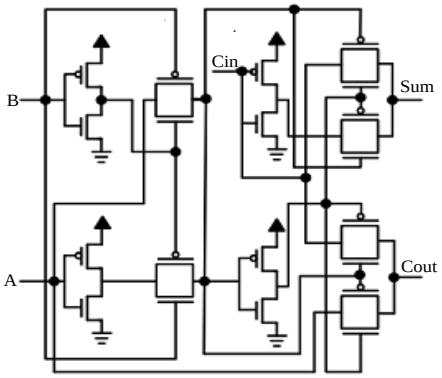


***Figure 2. TG-CMOS Full Adder Cell Presented in [11]***

The other full adder circuit is presented in [12] and its main body is only made of NMOS Pass Transistors. This circuit has outputs with full swings. Since Pass Transistor logic is exposed to voltage drop, using output inverters are essential for increasing driving capability. The application of these output inverters has advantages such as speed, full swing output and driving capability. But because of several intermediate nodes and static inverters, it has high power consumption. The circuit of this design is displayed in Figure3.

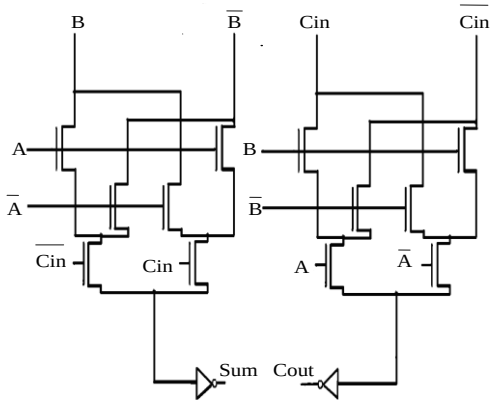


***Figure 3. CPL Full Adder Cell Presented in [12]***

NMNFA cell is proposed in [13] and is shown in Figure4. This design is implemented based on majority function. It includes 5 capacitors and 8 transistors. The critical path also consists of 3 transistors and 1 capacitor. Three different paths exist for producing Sum signals. The paths that are made up of MN and MP transistors have 2 transistor delays and the path that goes through transmission gates has a delay equal to 4 transistors.

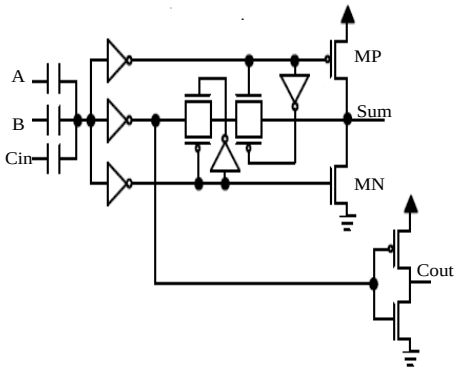


***Figure 4. NMNFA Cell Presented in [13]***

The next full adder cell to be studies here is MBFA full adder that is present in [14]. Its circuits are shown in Figure5. This design is implemented based on combination of minority function and bridge design. And include 3 capacitors and 16 transistors. The critical path of the circuits contains 4 transistors and one capacitor that lead to increase in output delay. Complement of Cout is created by a capacitor network and a CMOS inverter gate. Then, Sum output is created using Complement of Cout output and a bridge design.

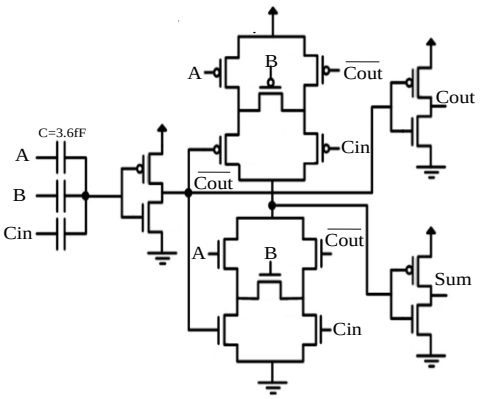


***Figure 5. MBFA Cell Presented in [14]***

A full adder cell based on XOR/XNOR is proposed in [15] that is shown in Figure6. This design includes 16 transistors. The critical path circuit includes 4 transistors. M1, M2, M3, M4, M5, M6, M7, and M8 transistors create XNOR and XOR functions and based on Sum and Cout outputs, the illustrated transmission gates will determine the proper logic for these outputs.

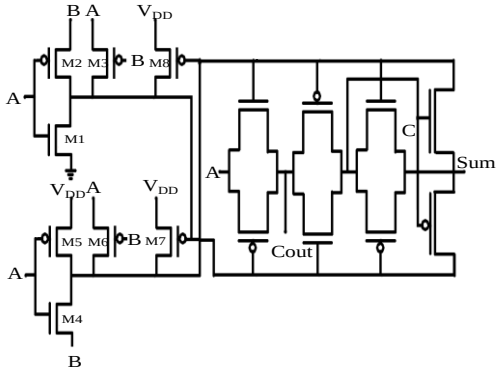


***Figure 6. XOR/XNOR-based Full Adder Cell Presented in [15]***

ULPFA cell circuit is presented in [16] and shown in Figure7. This design includes 30 transistors that lead to the increase in hardware overhead. The critical path of the circuit consists of 5 transistors. Cout and Sum outputs are created separately and independent from each other by two different circuits. Using inverters for Sum output to increase driving capability seems necessary. The delay in this circuit is relatively high. But the strong point of this design is its low power consumption.

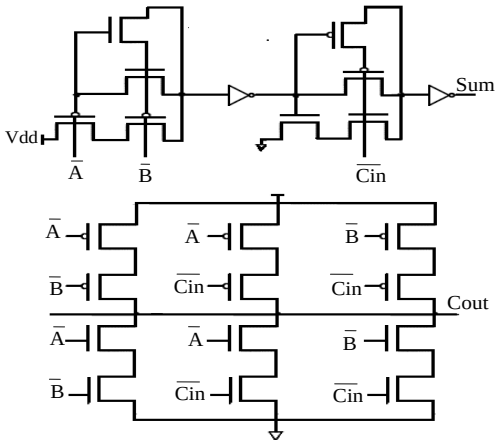


***Figure 7. ULPFA Cell Presented in [16]***

GDIFA cell circuit is presented in [17] and shown in Figure8. This design includes 18 transistors that lead to the decrease in hardware overhead. The critical path of the circuit consists of 4 transistors. Cout and Sum outputs are created separately and independent from each other by two different circuits. Using inverters for Sum and Cout output to increase driving capability seems necessary. The power consumption in this circuit is relatively low. But the strong point of this design is its low delay.

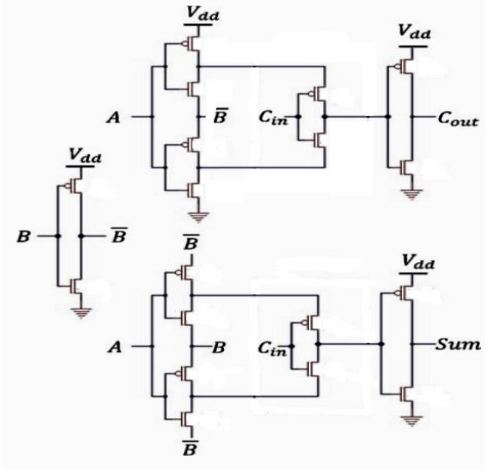


***Figure 8. GDIFA Cell Presented in [17]***

The next full adder cell to be studies here is HybridFA that is present in [18]. Its circuits are shown in Figure9. This design employed three different logic techniques: CCMOS, TG and PTL. And include 16 transistors. The critical path of the circuits contains 4 transistors.

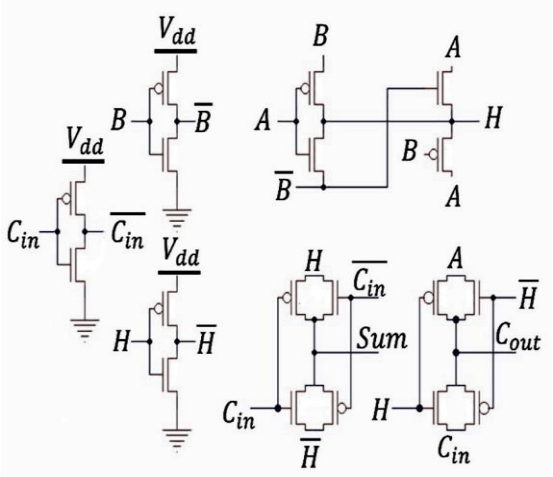


***Figure 9. HybridFA Cell Presented in [18]***

The last full adder cell that is discussed here is the full adder CLRCLFA proposed in [19]. The circuit of this full adder cell is depicted in Figure10. Contrary to former full adder cells discussed before, this circuit is based on CMOS technology. This model includes 12 transistors and the few number of transistors is considered an advantage for this design. The outputs do not have a full swing because of utilizing Pass Transistors causing low driving compatibility and long transmission delay.

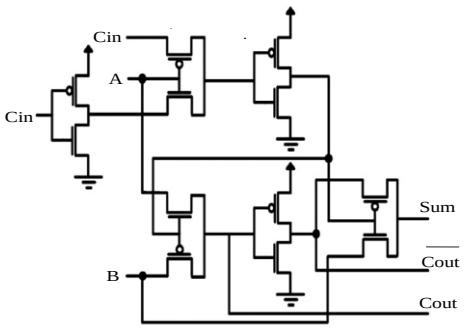


***Figure 10. CLRCL Full Adder Cell Presented in [19]***

## 3. Proposed Full Adder Cell

The proposed solution for reducing the delay of critical path in adder circuits is using a parallel structure in designing full adder cells. The structure of this parallel design is based on block diagram in Figure 11. In this structure, the addition of two input bits of A and B with 0 and 1, is calculated in a parallel and synchronously design. The Cin input bit determines which addition result should be carried to multiplexer gates. If Cin equals 0, then will be A+B+0, otherwise A+B+1 will be taken to the output.

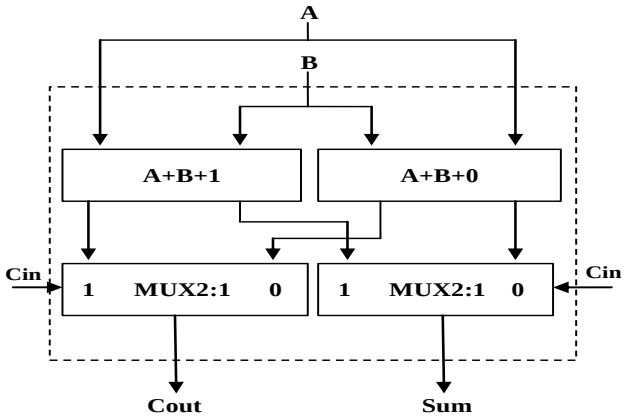


***Figure 11. The block diagram for the proposed full adder cell***

As it is shown in Figure 12, RCA circuits are implemented based on the proposed structure for full adder cells, after obtaining the Cin bit in each full adder except the first full adder, only required to one of Ai+Bi+0 or Ai+Bi+1 that were calculated before, transfer to the multiplexer output. Therefore, without any dependence on the delay of a full adder cell, the delay from the presence of each full adder cell on the critical path of the adder circuit will be equal to the delay of a multiplexer 2 to 1. Hence, in the n-bit RCA circuit based on the proposed structure, the delay of the critical path will be equal to the delay one full adder cell and (n-1) multiplexer 2 to 1.

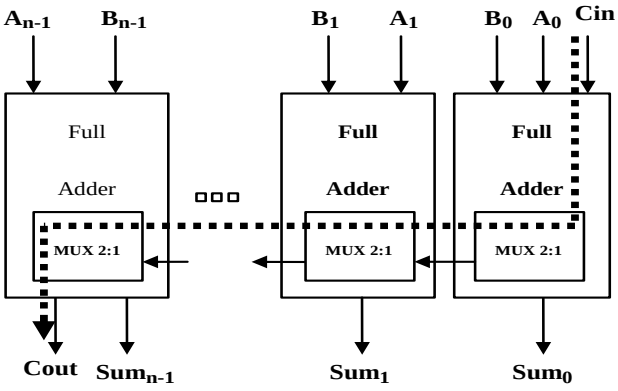


***Figure 12. n-bit RCA block diagram based on the proposed design***

In order to design a full adder cell based on parallel structure in Figure 11, some equations should be extracted for the Cout and Sum outputs so that their input Cin should be a determining one. This means that regarding the amount of Cin bit (0 or 1) we should be able to determine what relationship exists between A and B inputs to supply the proper logic for Cout and Sum outputs. We are going to make use of table 1 to obtain these equations. Based on this table, if Cin=0, then the Sum output will be equal to and if Cin=1 then the Sum output will be equal to . Therefore, Cin can determine the Sum output. Likewise, for the output Cout, if Cin=0, then the Cout output equals (A.B), and if Cin=1, then the Cout output will be equal to (A+B). So, Cin can determine the amount of Cout output. According to the explanations here, equations (3) and (4) for Cout and Sum will be as follows:

$$\text{Sum} = \overline{\text{Cin}}.\left[\overline{(\text{A}.\text{B})}.(\text{A}+\text{B})\right] + \text{Cin}.\overline{\left[\overline{(\text{A}.\text{B})}.(\text{A}+\text{B})\right]} \quad (3)$$

$$\text{C}_{\text{out}} = \overline{\text{Cin}}.(\text{A}.\text{B}) + \text{Cin}.(\text{A}+\text{B}) \quad (4)$$

***Table 1. The true table for the proposed full adder cell***

| A | B | Cin | A.B | A+B | Cout | Sum |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

The circuit of proposed full adder cell at gate level based on equations (3) and (4) is shown in Figure 13 and its circuit at transistor level is shown in Figure 14. In this circuit, OR and AND circuits are designed based on transmission gates and NOT gates are designed based on CMOS logic. Using CMOS logic and transmission gates has the advantage of full swing outputs. In case the outputs have a full swing, they will have a higher driving capability that leads to high speed of data movement along the critical path in the adder circuit.

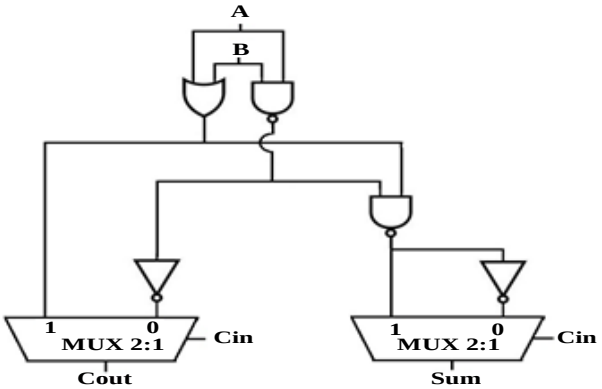


***Figure 13. Gate level circuit of the proposed full adder cell***

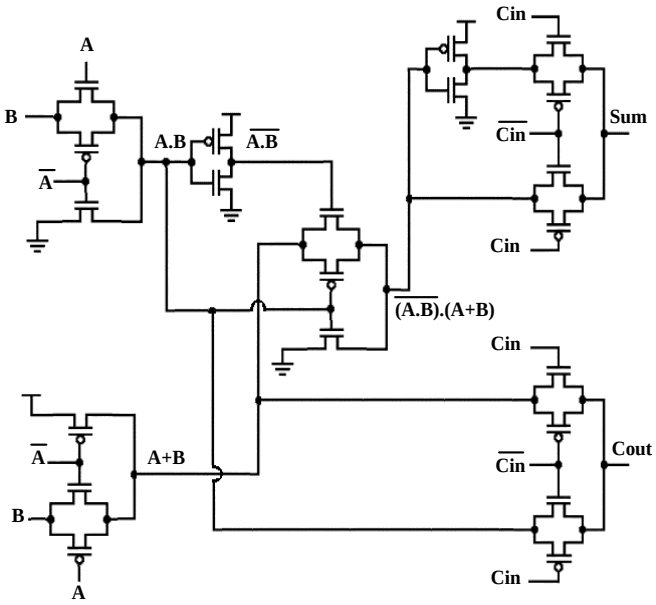


***Figure 14. transistor level circuit of the proposed full adder cell***

## 4. Simulation Results

A comprehensive simulation is carried out through the Synopsys HSPICE simulator software for the different environmental conditions in order to study and compare the efficiencies among different circuits. The circuits are simulated with 32nm CMOS technology.

PDP is specified as the main parameter for comparing the efficiency of different designs. The reason behind such an alternative is that this standard sets a compromise between power consumption and delay. The duration that the input reaches 50% level of power supply voltage is considered as the delay parameter till the output reaches the same voltage, too. Rising and falling propagation delays are separately calculated for Cout and Sum outputs, and the maximum amount is regarded as the delay parameter. Also, all the possible states of input passes to the circuit are implemented in order to calculate circuit delay. The delay of all outputs is considered for each pass and finally, the maximum delay will be reported as circuit delay. Power consumption is also the average power that is computed in during all the transistors. PDP parameter is obtained according to equation (5) which is the multiplication of the maximum delay and the average power consumption.

$$\mathrm{PDP} = \mathrm{Max}(\mathrm{Delay}) \times \mathrm{Avg}(\mathrm{Power\ Consumption}) \qquad (5)$$

Figure 15 shows required test pattern and output waveforms for the proposed full adder cell in 0.65 V power supply, 250 MHZ frequency, room temperature (25°C) and 2.1 fF load capacitance. This Figure indicates that the outputs are true and full swing. Simulation results are illustrated in table 2. The simulation results in different power

supply (0.5 volt, 0.65 volt, and 0.8 volt), are obtained with a capacitance of 2.1 fF and a room temperature conditions.

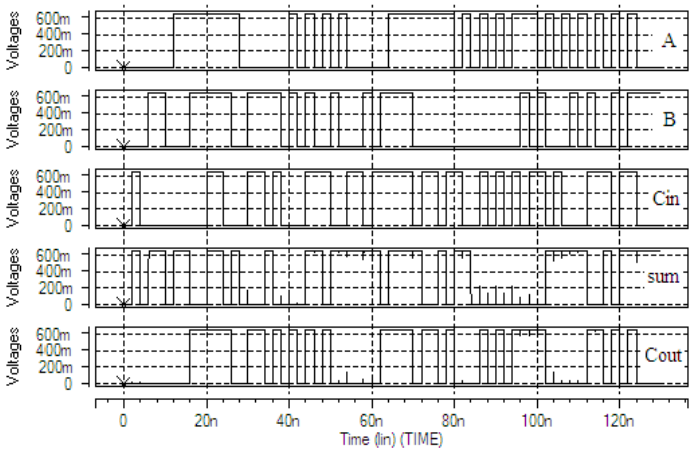


***Figure 15. Test pattern and output waveforms for proposed full adder cell***

***Table 2. Simulation results of the full adder cells***

| Full Adder Cells | Delay (pS) | Power (µW) | PDP (aJ) |
|---|---|---|---|
| **$V_{DD}$=0.8 v** | | | |
| CMOS-Bridge | 229.43 | 0.14922 | 34.236 |
| TG-CMOS | 283.39 | 0.16173 | 45.832 |
| CPL | 194.12 | 0.26124 | 50.711 |
| NMNFA | 340.92 | 0.51056 | 174.06 |
| MBFA | 128.93 | 0.34192 | 44.083 |
| XOR/XNOR-based | 157.19 | 0.18094 | 232.78 |
| ULPFA | 126.81 | 0.13317 | 16.887 |
| CLRCL | 744.13 | 0.51524 | 383.40 |
| GDIFA | 149.24 | 0.23562 | 35.166 |
| HybridFA | 115.64 | 0.34251 | 39.607 |
| Proposed FA | 117.91 | 0.20947 | 24.698 |
| **$V_{DD}$=0.65 v** | | | |
| CMOS-Bridge | 401.44 | 0.09815 | 39.401 |
| TG-CMOS | 557.09 | 0.10549 | 58.767 |
| CPL | 356.94 | 0.18124 | 64.691 |
| NMNFA | 571.63 | 0.28124 | 160.76 |
| MBFA | 189.27 | 0.20973 | 39.695 |
| XOR/XNOR-based | 193.47 | 0.14691 | 28.422 |
| ULPFA | 237.91 | 0.10091 | 24.007 |
| CLRCL | 1239.4 | 0.23891 | 296.10 |
| GDIFA | 197.04 | 0.18432 | 36.318 |
| HybridFA | 166.95 | 0.26254 | 43.831 |
| Proposed FA | 181.57 | 0.16937 | 30.752 |
| **$V_{DD}$=0.5 v** | | | |
| CMOS-Bridge | 1269.9 | 0.05732 | 72.793 |
| TG-CMOS | 2036.9 | 0.06590 | 134.24 |
| CPL | 970.02 | 0.16181 | 156.95 |
| NMNFA | 736.18 | 0.19248 | 141.69 |
| MBFA | 240.73 | 0.17305 | 41.658 |
| XOR/XNOR-based | 265.19 | 0.13497 | 35.792 |
| ULPFA | 769.34 | 0.08219 | 63.232 |
| CLRCL | 1475.5 | 0.19134 | 282.32 |

| | | | |
|---|---|---|---|
| GDIFA | 280.36 | 0.15365 | 43.077 |
| HybridFA | 253.14 | 0.20720 | 52.450 |
| Proposed FA | 254.79 | 0.13717 | 34.949 |

The ability of the true operation in different frequencies is one of the recent requirements of digital systems. Thus, the proposed design and other designs are simulated in different frequencies. The results of these simulations are depicted in Figure 16. These results are obtained at 0.65 V power supply, room temperature, 2.1 fF load capacitor and the specified range of frequency. According to this diagram, it is evident that PDP is lower in the proposed full adder compared to the other designs.

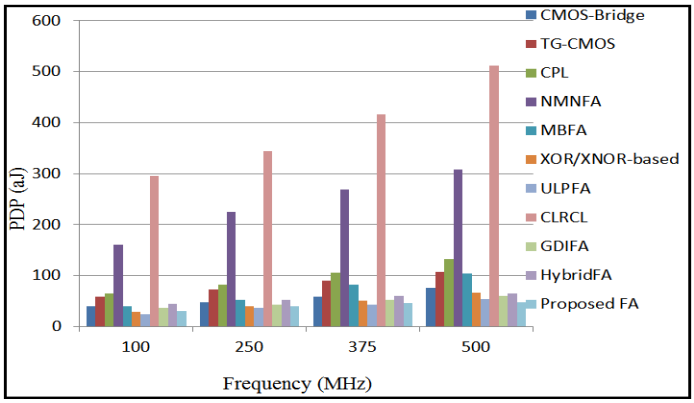


***Figure 16. PDP of full adders versus of different Frequency***

The driving capability is the speed that a circuit can charge or discharge circuit output. This circuit becomes more significant when it is exposed to high output capacity. In this state, it should have enough power to driving other circuits. Thereby, different circuits are evaluated at the presence of different load capacitors. The results of these simulations are shown in Figure 17. These results are obtained at 0.65 V power supply, 250 MHZ frequency, room temperature, and the specific range of load capacitors. As it is shown in this Figure, the proposed design is of acceptable efficiency in different output charges compared to the other designs.

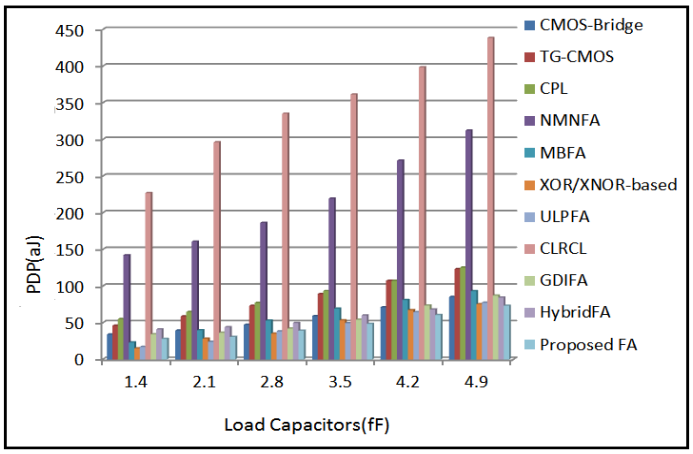

***Figure 17. PDP of full adders versus of Load Capacitors***

Since temperature noise negatively affects the efficiency of the designed circuits, it is one of the main concerns for circuit designers. Different circuits are simulated in different temperatures. The results of these simulations are shown in Figure 18. These results are obtained at 0.65 V power supply, 250 MHZ frequency, 2.1 fF load capacitor, and the specific range of temperatures. According to the results, it is evident that the performance of the proposed circuit is acceptable against different temperatures.

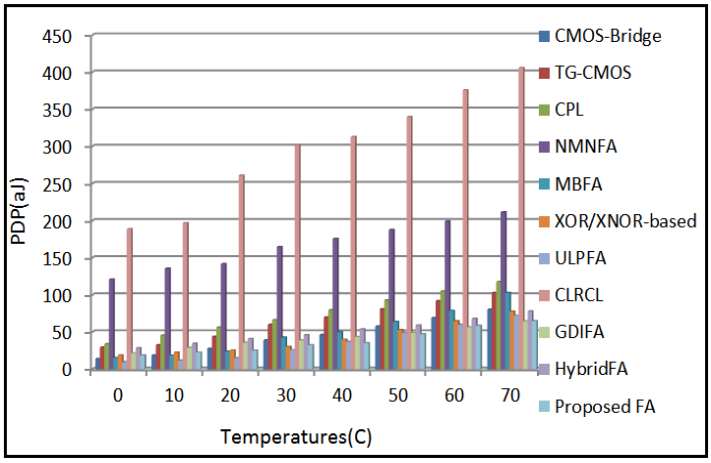


***Figure 18. PDP of full adders versus the different Temperatures***

Different circuits should possess this capability to be able to perform in larger circuits with a higher efficiency. Also, it is preferable that full adder cells that are in fact the adder be compared to each other. Therefore, 4 bit RCA and 8 bit RCA circuits are simulated based on the proposed full adder cells and other full adder cells. The results of these simulations are depicted in table 3 and table 4. According to the results it can be observed that the proposed design leads to a considerable improvement than other designs because of the shortening of the data path.

***Table 3. Simulation results of 4-bit adders***

| 4-bit RCAs | Delay (pS) | Power (µW) | PDP (a J) |
|---|---|---|---|
| CMOS-Bridge | 2035.23 | 0.23157 | 471.285 |
| TG-CMOS | 2256.72 | 0.39132 | 883.099 |
| CPL | 1894.86 | 0.64827 | 1228.38 |
| NMNFA | 3819.76 | 0.81648 | 3118.75 |
| MBFA | 885.776 | 0.71827 | 636.226 |
| XOR/XNOR-based | 739.156 | 0.61682 | 455.963 |
| ULPFA | 983.194 | 0.39346 | 386.859 |
| CLRCL | 5193.34 | 0.81943 | 4255.57 |
| GDIFA | 938.194 | 0.51942 | 487.316 |
| HybridFA | 695.325 | 0.92354 | 642.160 |
| Proposed FA | 439.713 | 0.68219 | 299.972 |

***Table 4. Simulation results of 8-bit adders***

| 8-bit RCAs | Delay | Power | PDP |
|---|---|---|---|

| | (p S) | (µ W) | (aJ) |
|---|---|---|---|
| CMOS-Bridge | 4138.59 | 0.6793 | 2811.50 |
| TG-CMOS | 5192.37 | 1.0118 | 5254.11 |
| CPL | 3952.91 | 1.9281 | 7621.60 |
| NMNFA | 7291.27 | 2.2097 | 16111.5 |
| MBFA | 1869.71 | 1.4025 | 2622.27 |
| XOR/XNOR-based | 1749.28 | 1.4872 | 2601.53 |
| ULPFA | 2108.35 | 0.8072 | 1701.90 |
| CLRCL | 12329.4 | 3.0194 | 37227.2 |
| GDIFA | 1838.79 | 1.0954 | 2014.21 |
| HybridFA | 1467.08 | 2.1425 | 3143.21 |
| Proposed FA | 915.664 | 1.1776 | 1078.28 |

## 5. Conclusions

A full adder cell based on CMOS technology has proposed. This cell can work in wide range of frequencies, load capacitors, and temperatures. The most salient advantage of the proposed full adder is the significant reduction of the data path delay in large adder circuits. Accordingly, the proposed design can be utilized in several applications, especially in arithmetic circuits that are for the purpose of high speed circuit.

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