A Low Power Full Adder Cell based on Carbon Nanotube FET for Arithmetic Units

Mokhtar Mohammadi Ghanatghestani1,2, Mehdi Bagherizadeh1,2

1) Department of Computer, Bam branch, Islamic Azad University, Bam, Iran
2) Department of Computer Engineering, Rafsanjan Branch, Islamic Azad University, Rafsanjan, Iran

mokhtarmohammadi@iaubam.ac.ir; m.bagherizadeh@srbiau.ac.ir

Received: 2019/01/19; Accepted: 2019/06/09

Abstract

In this paper, a full adder cell based on majority function using Carbon-Nanotube Field-Effect Transistor (CNFET) technology is presented. CNFETs possess considerable features that lead to their wide usage in digital circuits design. For the design of the cell input capacitors and inverters are used. These kinds of design method cause a high degree of regularity and simplicity. The proposed design can be used in many applications specifically wherever the low power consumption is the goal. The proposed full adder cell is compared to seven full adders in terms of power consumption, speed, power delay product (PDP), and Energy delay product (EDP). Also in order to evaluate the proposed design, several simulations are performed in different load capacitors, frequencies and temperatures. Simulation results demonstrate the higher efficiency of the proposed full adder cell with respect to other conventional and modern CNFET and MOSFET implementations. All Simulations are performed by using Synopsys HSPICE with 32 nm CMOS and 32 nm CNFET technologies.

Keywords: Carbon Nanotube Field Effect Transistor, Full adder, Low power, Majority function.

1. Introduction

Arithmetic circuits of digital computers play a major task in data processing. Addition operation is a major arithmetic function and another operation can be calculated based this operation. In most systems, the adder circuits specify the whole efficiency of the system. These instances are main goals for betterment adder circuits [1], [2]. Full adder is a cell which includes three inputs of A, B and Cin and shows the addition of these two bits by using the output of Sum and Cout through Sum + 2Carry = A+B+Cin equation. The relation between input and output is defined as equations (1) and (2) [3].

\[
\text{Sum} = A_i \oplus B_i \oplus C_{in} \quad (1)
\]

\[
C_{out} = A_iB_i + A_iC_{in} + B_iC_{in} \quad (2)
\]

The most important parameters in design and implementing the arithmetic circuits are hardware efficiency, speed and power consumption. Although lowering the supply voltage leads to reduce the power consumption, it increases the circuit delay. Hence, different designers are faced more constraints: low power consumption, high speed, and
high throughput [4]. By huge increasing of mobile and wireless applications which have limited the amount of power, circuits with low power consumption are more required. Low power design is suitable for microprocessor and system components [5], [6].

CNFETs are superior to MOSFETs in several reasons. The mobility of CNFET type n and p is equal. Thus, in comparison to MOSFET technology, it would be easier to determine transistor size in complex circuits based on CNFET technology. In addition, power consumption of CNFET is lower and their switching speed is much faster than MOSFETs [6]-[8].

The threshold voltage ($V_{th}$) of CNFETs is calculated by using equations (3) and (4). The $V_{th}$ of these transistors has inversely related to diameter of carbon nanotubes (DCNT). In these equations, $E_g$ represents the band gap, while $e$ is unit the charge of an electron, $a$ is the distance between two carbon atoms (0.249 nanometers), and $V_\pi$ (equal to 3.033 ev) is equivalent to carbon $\pi-\pi$ bond energy [9], [10].

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{a.V_\pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT} (nm)}$$ \hspace{1cm} (3)

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1n_2}}{\pi} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1n_2}$$ \hspace{1cm} (4)

The rest of this paper is structured as follows: previous works are reviewed in section 2; In Section 3, the proposed full adder cell is presented; Section 4 supplies the simulation results and comparison of the proposed design with other designs; and lastly, in section 5, the conclusions of this paper are provided.

2. Previous Works

The proposed full adder cell is compared to five, discussed full adder cells in this section. These full adders are selected in CNFET and MOSFET technologies.

The first full adder cell to be reviewed in this section is MBFA, presented in [11]. The circuit of this cell is shown in figure 1. This circuit is based on two methods, minority function and bridge style. This cell includes sixteen transistors and three capacitors. There are one capacitor and four transistors in the critical path. The Complement of Cout output is produced by means of the capacitor network and a not gate. Then, by using a bridge style sum output is produced.
The second full adder cell is CNFETFA-1 which was suggested in [12], and shown in figure 2. This circuit also produces the minority function by using capacitor network. This design includes twelve transistors and three capacitors. The outputs of this circuit are not full swing and have static power consumption due to the use of the Pass-Transistors.

The subsequent circuit is known as CNPTL. This circuit is proposed in [13] and is shown in figure 3. CNPTL full adder is consisted of twenty transistors, and its design is completely symmetric. The speed of this circuit is very high, due to the existence of only two transistors in its critical path. The power consumption of this circuit is relatively low, since the Sum producing circuit does not include any direct path between the power supply and GND. The outputs of this circuit are not full swing and have static power consumption due to the use of the Pass-Transistors.
A Low Power Full Adder Cell based on …  

The CNFETFA-2 full adder is our next circuit, which was proposed in [14] and is shown in figure 4. CNFETFA-2 is combination of three structures. The first structure creates XOR/XNOR gates. Then, the second and third symmetric structures are used to produce Sum and Cout outputs. This circuit has 28 transistors, and the critical path is consists of four transistors.

The CNFETFA-3 full adder is next circuit, which was proposed in [15] and is shown in figure 5. First complement of Sum and Cout signals are produced. Then using two inverter gates non complement signals are produced. Presence of inverters improves driving capability of this cell.
The CNFETFA-4 full adder is next circuit, which was proposed in [15] and is shown in figure 6. CNFETFA-4 is used of three gates. This circuit has 12 transistors and three capacitors, and the critical path consists of three transistors and one capacitor.

Finally, the last full adder cell to be reviewed in this section is CLRCLFA. And is presented in [17]. Figure 7 shows the design of this cell. In comparison with all the before circuits, the design of this cell is based on CMOS technology. One of the benefits of this design is the low number of transistors. The outputs are not full swing since Pass-Transistors are used. And can cause low driving capability and long propagation delay.
A Low Power Full Adder Cell based on … M. Mohammadi Ghanatghestani, M. Bagherizadeh

3. Proposed Full Adder Cell

In this chapter a full adder cell based on the Majority function is proposed. In this design, Majority function is implemented by use of three capacitors and two static inverters (Figure 8) [17].

![Proposed Full Adder Cell](image)

Figure 7. CLRCLFA Full Adder Cell Presented in [17]

![Three-Input Majority gate](image)

Figure 8. Three-Input Majority gate

Cout is equal to a three-input Majority function. And this property is specified in Table 1. Therefore Cout can be calculated by the equation (5).

\[
Cout = \text{Majority} (A, B, Cin)
\]  

(5)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Cin</th>
<th>Maj(A, B, Cin)</th>
<th>Cout</th>
<th>Sum</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1. Full Adder Truth Table

sum can be calculated by the following equation (6).
The proposed full adder cell is implemented based on Equations (5) and (6). The circuit of this full adder is shown in Figure 9. Implementing the proposed design is composed of two sections. The first section is an array of capacitors which computes addition of voltages A, B, and Cin signals. Therefore, voltage of Vx in Figure 9 includes four levels of voltage: 0v, Vdd/3, 2Vdd/3, and 3Vdd/3=Vdd. The first stage implements Cout by means of a majority function. second stage utilizes a seven-input majority function to implement sum. Three of its inputs (A, B and C) are similar to the previous stage. One input is created by using the previous stage output (Cout). Other three inputs are created by using the previous stage output (complement of Cout). If more than three inputs are high the sum output will increase to '1'. Otherwise the sum output will reduce to '0'.

\[
\text{Sum} = \text{Majority}(A, B, \overline{\text{Cin}}, \overline{\text{Cout}}, 3^* \overline{\text{Cout}}) = \text{Majority}(A, B, \overline{\text{Cin}}, \overline{\text{Cout}}, \overline{\text{Cout}}, \overline{\text{Cout}}, \overline{\text{Cout}}) = \\
A \cdot B \cdot \overline{\text{Cin}} \cdot \overline{\text{Cout}} + A \cdot \overline{\text{Cout}} + B \cdot \overline{\text{Cout}} + \text{Cin} \cdot \overline{\text{Cout}} + \text{Cout} \cdot \overline{\text{Cout}} = \\
A \cdot B \cdot \overline{\text{Cin}} \cdot (A \cdot B + A \cdot \overline{\text{Cin}} + B \cdot \overline{\text{Cin}}) + A \cdot (\overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{\text{Cin}} + \overline{B} \cdot \overline{\text{Cin}}) + B \cdot (\overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{\text{Cin}} + \overline{B} \cdot \overline{\text{Cin}}) + \\
\text{Cin} \cdot (\overline{A} \cdot \overline{B} + \overline{A} \cdot \overline{\text{Cin}} + \overline{B} \cdot \overline{\text{Cin}}) + (A \cdot B + A \cdot \text{Cin} + B \cdot \text{Cin}) \cdot (\overline{A} \cdot \overline{B} + A \cdot \text{Cin} + B \cdot \text{Cin}) = \\
A \cdot B \cdot \overline{\text{Cin}} + A \cdot \overline{B} \cdot \overline{\text{Cin}} + A \cdot B \cdot \text{Cin} + A \cdot \overline{B} \cdot \text{Cin} = \text{XOR}(A, B, \text{Cin})
\]

\( (6) \)

The proposed full adder cell works properly in different supply voltages with minimum power consumption, specifically dynamic power consumption. Also Power delay product in this design is very low. By using this method the number of transistors is reduced. Therefore, the proposed circuit is the most hardware efficient Full Adder compared to other designs. In this circuit, symmetry property is also another important advantage.

4. Simulation Results

The In this section the proposed full adder cell is compared to other full adder cells discussed in section 2. The performances of different circuits were evaluated and compares by means of Synopsys HSPICE simulation software which provided a comprehensive simulation based on different conditions. The 32 nanometer model was
used for CMOS based circuits, while the 32 nanometer model proposed in [18] and [19] was considered for CNFET based circuits. The most important parameters of this model and their brief description are mentioned in table 2.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(L_{ch})</td>
<td>Physical channel length</td>
<td>32 nm</td>
</tr>
<tr>
<td>(L_{geff})</td>
<td>Mean free path in the intrinsic CNT channel</td>
<td>100 nm</td>
</tr>
<tr>
<td>(L_{ss})</td>
<td>Length of doped CNT source-side extension region</td>
<td>32 nm</td>
</tr>
<tr>
<td>(L_{sd})</td>
<td>Length of doped CNT drain-side extension region</td>
<td>32 nm</td>
</tr>
<tr>
<td>(K_{gate})</td>
<td>The dielectric constant of high-k top gate dielectric material</td>
<td>16</td>
</tr>
<tr>
<td>(T_{ox})</td>
<td>The thickness of high-k top gate dielectric material</td>
<td>4 nm</td>
</tr>
<tr>
<td>(C_{sub})</td>
<td>The coupling capacitance between the channel region and the substrate</td>
<td>40 pF/m</td>
</tr>
<tr>
<td>(E_{fi})</td>
<td>The Fermi level of the doped S/D tube</td>
<td>6 eV</td>
</tr>
</tbody>
</table>

In comparing different designs, PDP was chosen as the main comparative parameter, since PDP forms a kind of compromise between power consumption and delay. The amount of input needed for power supply voltage to reach 50% until the time when output reaches the same voltage is considered as the delay parameter. Rising and falling propagation delay is separately calculated for Sum and Cout outputs and the maximum value is considered as the delay parameter. In addition, all possible transition inputs are applied to the proposed circuit in order to calculate circuit delay. Delay of all outputs for each transition is considered and, eventually, the longest delay is reported as circuit delay. Power consumption is in fact the average consumed power which is calculated during long periods of time. PDP parameter is calculated based on equations (7).

\[
PDP = \text{Max}(\text{Delay}) \times \text{Avg}(\text{Power Consumption})
\]

Figure 10 shows the input and output waveforms for the proposed circuit with 0.65v power supply, and 2.1 fF load capacitance. According to this figure, all outputs are correct and are full swing. Simulation results are shown in table 3. These simulation results are obtained with different power supply (0.5v, 0.65v and 0.8v), 2.1 fF load capacitance and room temperature of 27°C.
Different circuits should possess this capability to be able to perform in various frequencies. Hence, the different circuits were simulated at various frequencies. The simulation results are specified in the diagram of figure 11. These simulations were performed with room temperature, 2.1 fF load capacitor, 0.65v power supply, and specified range of frequency.
Figure 11. PDP of full adders versus of different Frequency

The driving capability of a circuit is the speed that it can charge or discharge its outputs. Different circuits should be strong enough to start other circuits as well. Therefore, different circuits were simulated in various Load Capacitors. Results of these simulations are specified in the diagram of figure 12. These simulations were performed with room temperature, 250 MHz frequency, 0.65v power supply, and output load capacitor with defined variation range.

Figure 12. PDP of full adders versus of Load Capacitors

To evaluate the circuits operation at different temperatures, all circuits are simulated in different temperatures. Results of these simulations are specified in the diagram of figure 13. These simulations were performed at 2.1 fF load capacitor, 250 MHz frequency, 0.65v power supply, and the specific range of temperatures.

Figure 13. PDP of full adders versus the different Temperatures
5. Conclusions

A novel low-power Majority function-based single-bit full adder cells have been proposed. The proposed full adder uses capacitance and inverter in its structure resulting in a significant very reduction in power consumption, specifically dynamic power consumption. Some techniques to improve the power consumption of the circuit resulted in this new adder benefiting from the best PDP and high performance. The proposed design was capable of working perfectly in different vast range of temperature and different Frequency. Finally, this new circuit is appropriate to be applied for construction of large low-power high performance VLSI systems.

References


A Low Power Full Adder Cell based on …  

M. Mohammadi Ghanathestani, M. Bagherizadeh


