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A New Design for Two-input XOR Gate in Quantum-dot Cellular Automata

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Abstract

Quantum-dot Cellular Automata (QCA) technology is attractive due to its low power consumption, fast speed and small dimension, therefore, it is a promising alternative to CMOS technology.In QCA, configuration of charges plays the role which is played by current in CMOS. This replacement provides the significant advantages. Additionally, exclusive-or (XOR) gate is a useful building block in many important circuits such as full adder (FA). In this paper we propose a novel design for two-input XOR gate in QCA. Two-input XORs could be utilized in constructing three-input ones which are widely used. The proposed XOR gate is the smallest design among the two-input XORs and it achieves significant improvements in terms of complexity and latency in comparison to the only existing similarlydesigned gate. Contrary to the common designingmethod which uses the logic functionof XOR, the gate is constructed based on explicit interactions between QCA cells.The simulation results have been verified using the QCADesigner.

Keywords:*Quantum-Dot Cellular Automata (QCA), Nanotechnology, Circuit Design, XOR gate, Circuit Simulation.*

1. Introduction

Nowadays conventional CMOS technology faces serious challenges such as physical limits, high power consumption, short channel effects and low speed. These disadvantages affect negatively on the reliability of CMOS devices. Hence the deficiencies have resulted in an increase in the number of researches in new technologies at nanoscale in recent years [1]. Quantum-dot Cellular Automata (QCA) is one of the promising alternatives which is attractive due to its low power consumption, fast speed and small dimensions. The basic QCA cell consists of four quantum dots with two free charges which can only tunnel between the dots. Unlike the conventional CMOS, the QCA is a binary logic based architecture which encodes binary information rather than using current and therefore it can minimize logical circuits in nanoscale designs which operate at very low power levels without any current leakage. Due to Coulombic interactions between electrons in Quantum Dots, two stable states might occur which are encoded to logic “0” and logic “1” [2-4].

QCA gates and circuits can be realized by an array of QCA cells. The accuracy of operations in QCA circuits is determined by the locations of the cells, thus in order for the circuits to function properly, the cells must be correctly aligned. In this paper, we

present a novel QCA design for two-input XOR gate which might be used in constructing some other useful QCA gates and circuits.

The rest of this paper is organized as follows. In section 2, a review of the QCA is presented. Section 3 explains clocking in QCA. In section 4 the proposed XOR gate is given. Structural analysis and the related comparisons are presentedin section 5. Section 6 shows the simulation result. Finally, section 7 concludes the paper.

2. Review of QCA

A QCA cell is composed of four quantum-dots positioned at the corners of a square. These dots can be occupied by two identical mobile charges. If the potential barrier which separates the dots is low, electrons can quantum- mechanically tunnel between dots, but they are not permitted to leave the cell. Due to the Coulombic repulsion between the charges, they will tend to occupy diagonally the opposed dots. This feature leads to two possible stable configurations which are represented as cell polarizations P=-1 and P=+1. Accordingly the binary values "0" and "1" can be encoded in polarizations -1 and +1, respectively [2-4]. This concept is illustrated in Figure 1.

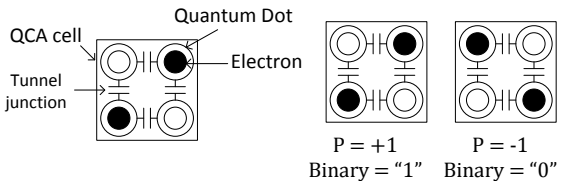

Figure 1. QCA cell and two possible polarizations.

Logic operations are performed by dint of Coulombicinteractions between adjacent cells [2, 4]. The 90-degree wire, Figure 2(a), is a row of cascaded QCA cells which propagate binary signal from input to output. Electron repulsion between the cells will cause the change of their polarization to one of the right ground states. Other than the 90-degree QCA wire, 45-degree wire is used for coplanar wire crossings and alternates binary signal polarization in consecutive cells as shown in Figure 2(b) [5]. The fundamental QCA logic gates are the inverter and the majority gate [6, 7] which most circuits have been implemented based on [8-14]. These gates are shown in Figure 2(c) and 2(d). An inverter, Figure 2(c), can be made up of wires. Initially, the input is split into two wires and at the end these wires are returned together by use of a 45-degree wire. The cell of the 45-degree wire produces a polarization in contrast with those in the two wires. In 3-input majority gate, as illustrated in Figure 2(d), the central cell owing to electrostatic repulsion between the electrons of the input cells, is polarized to the majority polarization and this polarization is then propagated as the output. Recently, some designs for 5-input majority gate have been suggested in [13, 14]. 5-input majority gate based realizations offer some improvements in terms of delay, occupied space as well as number of cells needed [13, 14]. Figure 2(e) illustrates two models proposed for 5-input majority gate. By fixing the polarization of one (two) of the three (five) inputs as logic "1" or logic "0", a 2(3)-input OR gate or a 2(3)-input AND gate can be obtained, respectively.

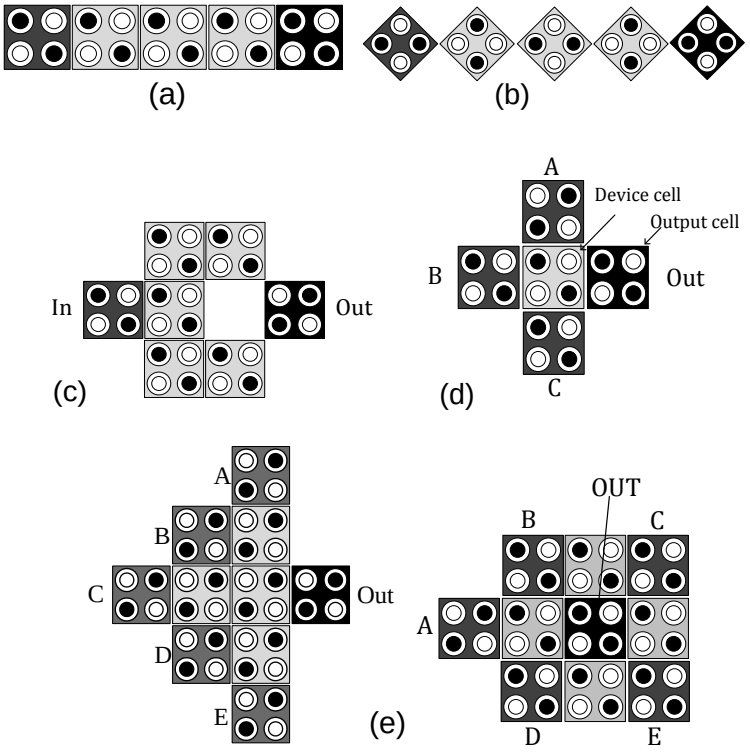

Figure 2. (a) 90-degree QCA wire, (b) 45-degree QCA wire, (c) An inverter, (d) A 3-input majority gate, (e) Two types of 5-input majority gate.

3. QCA clocking

Clocking in QCA circuitry is different from CMOS. The synchronization in QCA is accomplished by defining four distinct and periodic clocking zones which enable the QCA cells to pass the applied input to the desired output. In order to control each zone correctly, four clock signals are employed where each signal is shifted by 90° compared to the clock of the previous zone.

Each cell could be in one of four phases in accordance to the clock signal.

As shown in Figure 3 when clock is low the affected zone is in Relax phase in which the cells are unpolarized. At the rising edge and the high level, the zone is in Switch phase and Hold phase, respectively. The polarization process begins within the Switch phase and when the clock reaches the Hold phase, the zone is polarized completely. At the falling edge in which the corresponding zone is in Release phase, the polarization reduction occurs. After a clock, the input has propagated among the cells and is transferred to the end of the zone and this procedure can be carried out through the next quadruple zones. Hence inherent pipelining is provided in QCA clocking by the structure of discussed pipelined zones. The propagation delay of each QCA circuit is determined by the number of zones in its critical path [14, 15].

Since each clocked QCA zone get latched and remain latched until the next zone switches to Hold state, it acts as a D-latch and the QCA wire acts as a set of cascaded D-latches. The clocking mechanism provides synchronization as well as signal energy restoration [16]. This restoration which is achieved by the applied clock signals compensates the attenuation as data goes forward through the cells and makes the QCA circuitry significantly more fault tolerant.

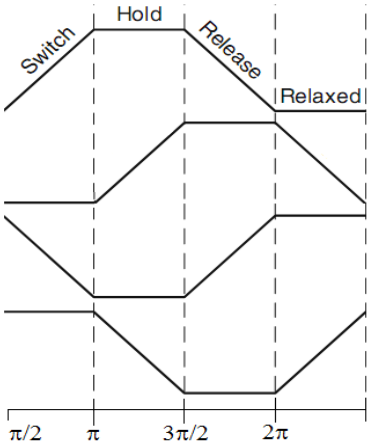

Figure 3. Four-phased clocks of the QCA zones.

4. Proposed approach

Two-input exclusive-or (XOR) gate is one of the widely used gates in QCA area [18-22]. It is utilized in constructing several QCA gates such as three-input XOR which is usually made up of two two-input XORs as shown in Figure 4. Hence, designing efficient QCA two-input XORs has a significant effect on complexity of larger circuits.

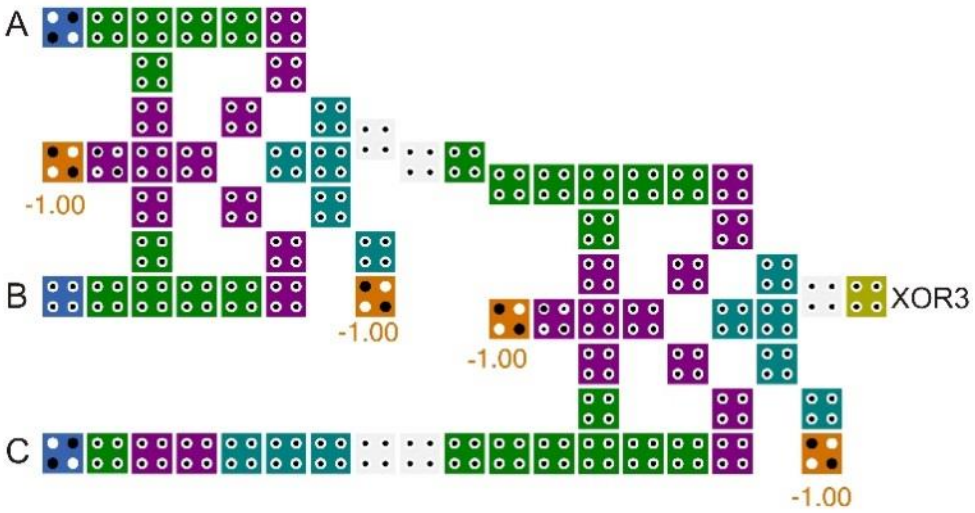

Figure 4. Conventional QCA implementation of a 3-input XOR gate using cascaded 2-input XORs based on the module presented in [23].

Most of the two-input XORs are designed based on the logic formula of XOR function [23].However, the output of the two-input XOR gate proposed in this paper is generated using explicit interactions between QCA cells. In other words, the presented gate is not implemented based on the logic formula.Figure 5 depicts the layout of the proposed two-input XOR gate. As depicted, the gate is composed of only 8 cells which is the lowest number of cells among the designs published up to now.

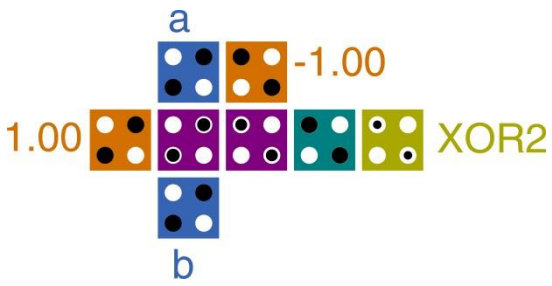

Figure 5. Layout of the proposed two-input XOR gate.

5. Structural analysis and comparisons

In order to investigate the efficiency of the proposed design for two-input XOR gate, it is compared with the XOR gate presented in [24] in terms of cell count (complexity), area and latency. Figure 6 shows the two-input XOR gate proposed in [24].

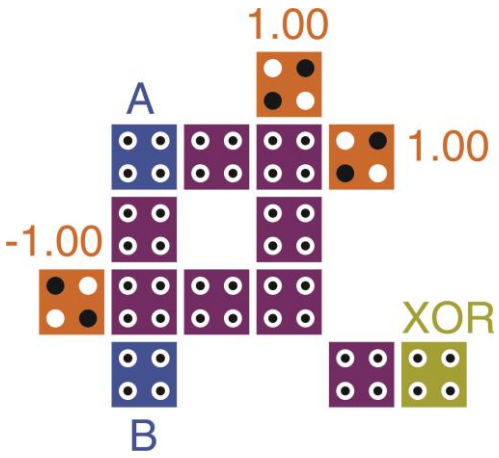

Figure 6. The two-input XOR gate presented in [24].

Table 1 summarizes the comparison factors of the two XOR gates. As it is clear, our gate achieves 42% and 50% improvements in terms of cell count and area, respectively.

Table 1. Structural analysis of the two-input XOR gates.

Circuit	Cell count (complexity)	Area (μm^2)	Latency (clock cycle)
Our proposed XOR	8	0.005	0.75
The XOR gate in [24]	14	0.01	0.5

6. Simulation result

In order to verify the function of the proposed XOR gate,QCADesigner cad tool is leveraged [17]. The following parameters are used for a bistable approximation: cell size=18nm, number of samples=50000, convergence tolerance=0.0000100, radius of effect=65.000000nm, relative permittivity=12.900000, clock high=9.800000e–022 J, clock low=3.800000e–023 J, clock shift=0, clock amplitude factor=2.000000, layer separation=11.500000 and maximum iterations per sample=100. Most of the above mentioned parameters are default values in QCADesigner. Figure 7 shows the simulation result of the proposed two-input XOR gate.

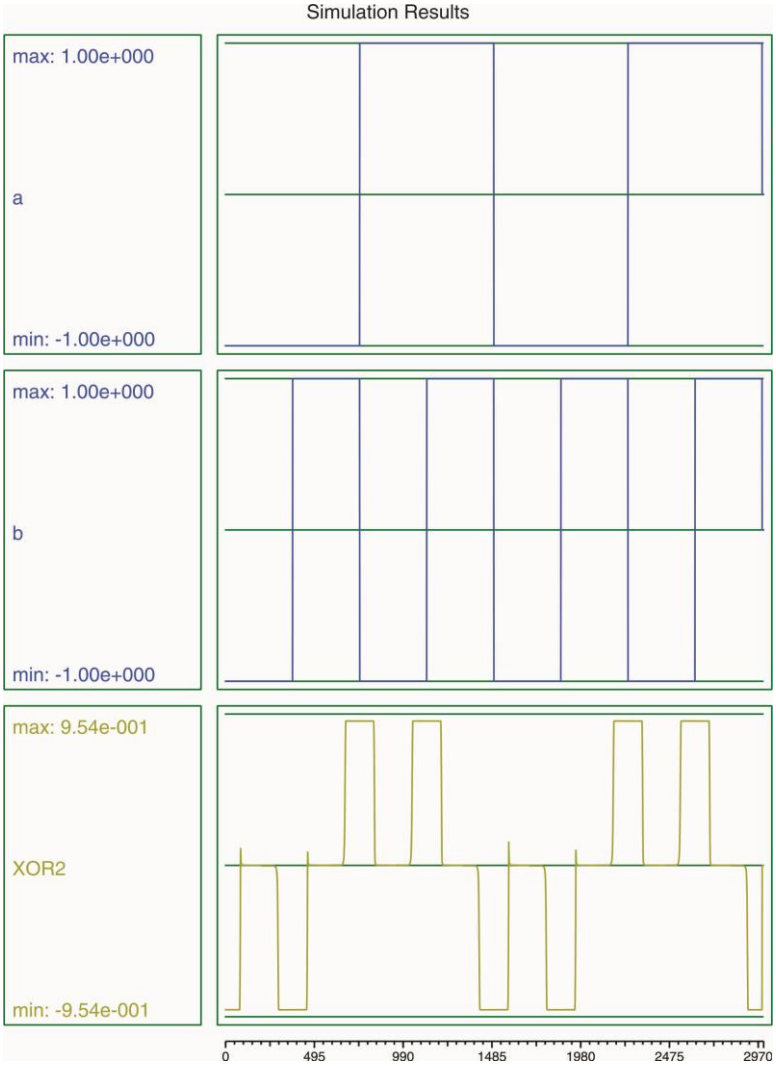

Figure 7. Simulation results of the proposed XOR gate.

7. Conclusion

Two-input XOR gate is extensively used in constructing large QCA circuits. This paper presents a robust design for two-input XOR gate. The gate generates the desired output utilizing explicit interactions between QCA cells rather than using a logic formula.As is clear, the gate is made up of only 8 cells,therefore, it is very small compared to the other designs. The results show that the XOR gate achieves 42% and 50% improvements in terms of cell count (complexity) and area, respectively in comparison to the only similar existing design.

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