A novel design for all-optical NAND/NOR/XOR gates based on nonlinear directional coupler

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Abstract

In this paper a novel all-optical logic NAND, NOR and XOR gate based on nonlinear directional coupler theory is demonstrated. We use the identical structure which contains three waveguides, for designing these gates; the only difference however, is the power of inputs light beam. In other words, while a beam with 4 W/µm in power considered as logical one, the output is NAND gate and if a beam with 6 W/µm in power considered as logical one, the same output, will be represented, the NOR function. In this case, an other waveguide of the structure is represented the XOR gate. Therefore this case, shows both NOR/XOR gates simultaneously. By use of three waveguides and adjusting the refractive index of waveguides and selecting the proper waveguide length, NAND/NOR/XOR gates can be obtained. The operation of these gates is simulated by use of Rsoft's BeamPROP simulator.

Keywords: *All-optical gates, Coupling, Nonlinear directional coupler, Refractive index, Waveguide*

1. Introduction

All-optical signal processing techniques are rapidly increasing due to its capabilities for the development of high-speed and high-capacity telecommunication systems [1]. All optical logic gates are the key element to perform optical signal processing such as optical bit pattern recognition addressing, parity checking, header recognition, data encoding, demultiplexing and switching with very high speed [2]. So far, several scheme have been suggested for various all-optical logical functions designing by means of four wave mixing (FWM) [3], semiconductor optical amplifier (SOA)[4], cross-polarization modulation[5], Terahertz Optical Asymmetric Demultiplexer [6] and Ultrafast Nonlinear Interferometer [7]. In recent years, many schemes reported to design of all optical NAND/NOR/XOR gates [8-13]. For example, the authors of [8] used nonlinear vertical-cavity semiconductor gates based on saturable absorption in semiconductor quantum wells to design NAND and NOR logical gates. The design of XOR, NOR and NAND gates using two parallel semiconductor optical amplifier (SOA)-Mach–Zehnder interferometer (MZI) structures reported by Kim and his co-workers [9]. Also NAND, NOR and XOR logic gates constructed by combining cross-waveguide geometries including photonic crystal nonlinear cavity are proposed in [10].

In this paper we propose all-optical NAND/NOR/XOR logical gates based on nonlinear directional couplers (NLDCs) these schemes with NLDCs is simpler than other devices and also can be used for ultra-fast logical gates and switches [14]. NLDCs are important components in optical fiber telecommunication systems and all integrated optical circuits. In our work, the operation of all-optical NAND/NOR/XOR logical gates is achieved by means of three waveguides and coupling theory.

2. Design and simulation results

NAND, NOR and XOR gates are basic logic gates; NAND and NOR are called "universal gates" because all of the other gates can be constructed using only those two gates. In fact, in chips, entire logic maybe built using only NAND (or NOR) gates. The output of NAND gate is high when either of inputs A or B is high, or if neither is high; it is going low only if both A and B are high. The output of NOR gate is high if both of the inputs are low and otherwise it's low. The output of XOR gate is high if either, but not both, of its two inputs are high. The truth table of NAND/NOR and XOR gates is shown in table 1.

Table 1. Truth table of NAND, NOR and XOR gates

Input		NAND	NOR	XOR
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	0	0

2.1 Concept of coupled-mode theory

In this section, the basic principle of waveguide coupling is presented and discussed using mathematical principles. If the waveguides are sufficiently close each other, mutual coupling will be occurred. In other word, light beam can be transferred between the waveguides and total power or partial power can be exchanged between them as shown in Figure 1.

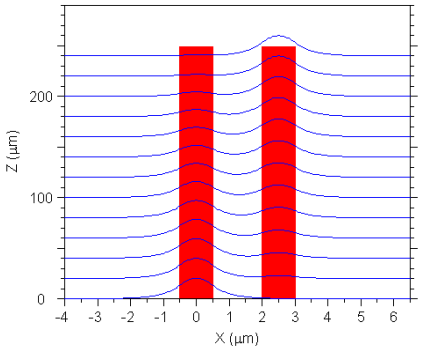


Figure 1. Coupling between two parallel waveguides

The coupled equations for the field amplitude in each waveguide are written as [15- 16]:

$$\frac{da_1}{dz} = -jk_{21}\exp(j\,\Delta\beta\, z)\, a_2(z) \qquad (1)$$

$$\frac{da_2}{dz} = -jk_{12}\exp(-j\,\Delta\beta\, z)\, a_1(z) \quad (2)$$

In above equations, $\Delta\beta_1 = \beta_1 - \beta_2$ is the phase mismatch per unit length and $a_1(z)$ and $a_2(z)$ are amplitudes of the modes of waveguides 1 and 2 respectively. Also k_{21}, k_{12} are coupling coefficients in each waveguide and can be obtained as follows:

$$k_{21} = \frac{1}{2}(n_2^2 - n^2)\frac{k_0^2}{\beta_1}\int_a^{a+d} u_1(y)u_2(y)\, dy \quad (3)$$

$$k_{12} = \frac{1}{2}(n_1^2 - n^2)\frac{k_0^2}{\beta_2}\int_{-a-d}^{-a} u_2(y)u_1(y)\, dy \quad (4)$$

In which n1 and n2 are refractive indices for each waveguide which are embedded in a medium with refractive index n. A power transfer ratio that is expressed as a P2/P1 can be written as following equation:

$$\mathcal{T} = \left(\frac{\pi}{2}\right)^2 \mathrm{sinc}^2\left\{\frac{1}{2}\left[1 + \left(\frac{\Delta\beta\, L_0}{\pi}\right)^2\right]^{1/2}\right\} \quad (5)$$

Where P1 and P2 are powers at the end of waveguides 1 and 2 respectively and L_0 is coupling length. The power transfer ratio depends on the mismatch parameter $\Delta\beta L_0$ as shown in Figure 2.

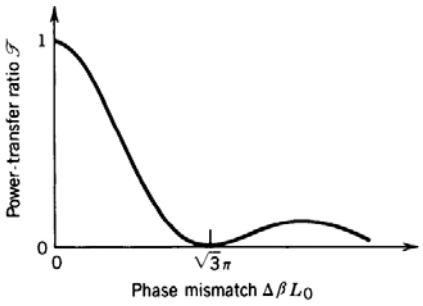


Figure 2. Power transfer ratio vs. Phase mismatch.

In a Kerr-type material, the refractive index, n, is described by the Kerr law, $n = n_0 + n_2 I$, where n_0 is the linear refractive index, n_2 is the third-order nonlinear coefficient, and I is the field intensity.

2.2 NAND, NOR and XOR gates design

For designing the logic NAND, NOR and XOR gates we use three waveguides, one of them has nonlinear behavior and two of them are linear guides. The operation of these gates will be obtained by using coupled-mode theory, adjusting the refractive indices of waveguides, selecting the proper length and width of guides, and adjusting the gap between waveguides. The proposed structure is depicted in Figure 3. In this scheme, the same structure is used to design of logic NAND, NOR and XOR gates. For this purpose, when we use the light beam with 4 w/μm in power as logical one, the end of the waveguide 3 is represented NAND gate; and when the logical one is the light beam with 6 w/μm in power, the function of NOR gate will be obtained from the same channel (the end of the waveguide 3) in this case, the end of the waveguide 1 shows XOR gate; in other words in this situation we have the operation of both NOR and XOR gates simultaneously.

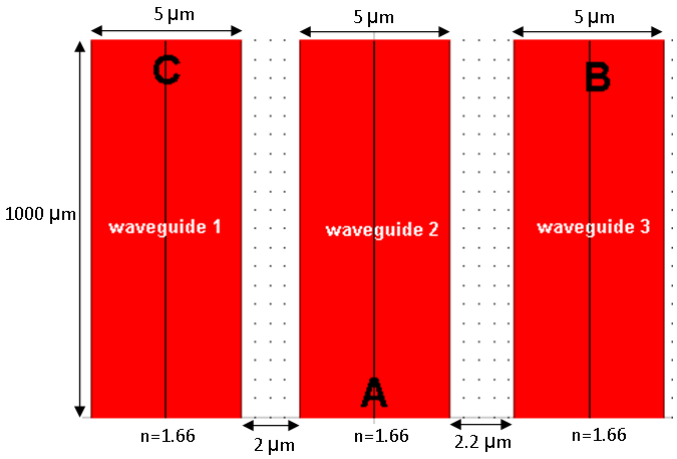


Figure 3. Proposed structure of all-optical logic NAND/NOR/XOR gates

In this structure, the PTS (n0 = 1.66 and n2=2 ×10-4 µm2/W) is used for waveguide 2 which is nonlinear medium and refractive indices of the waveguide 1 and 3 are set to 1.66 which are linear mediums. In fact, the refractive indices of linear mediums, waveguide 1 and 3, set to this value by the aid of equivalent layers theory. By using of this theory, the linear mediums with any arbitrary refractive index can be achieved [17]. In our scheme only the waveguide 2 shows nonlinear behavior. It means that the refractive index of this waveguide will be changed by the input light; the amount of change is depending on the input light intensity. Waveguide 1 and 3 have a linear behavior and their refractive indices will be remained constant when the light passes through them. This structure has three ports naming as A, B and C. Where the A port is considered as input port and all inputs are applied to this port synchronously. Also B port is the output of NAND and NOR gates and the C port is representing the output of XOR gate only when logical one is the light beam with 6 w/µm power.

In NAND and NOR gates when both of inputs is logical zero, the output of these gates should be logical one according to table 1. In optical design, it means that when there is no light in input, the output must has light, hence we need a control signal for providing this state of inputs. For this aim, a light beam is launched in waveguide 1 continuously, the power of this control beam is equal to the power of logical one, it means that for NAND gate this control beam is 4 w/µm in power and for NOR/XOR gate is 6 w/µm in power.

As mentioned before, this structure operates in two modes:

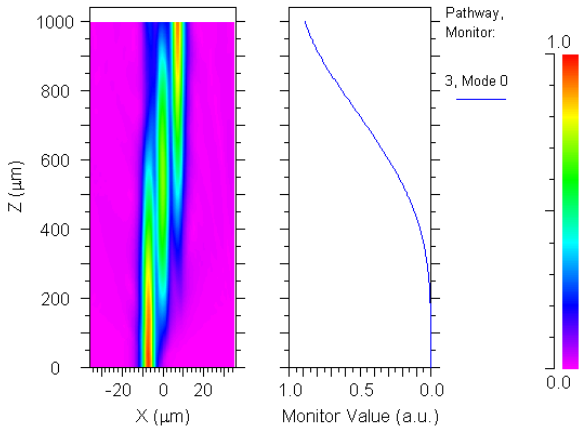
Logical one is equal to 4w/µm. In this mode, the control light is 4w/µm in power and launched into the waveguide 1 consistently; all input light beams are applied to A port synchronously. The B port is represented the NAND gate.

Logical one is equal to 6w/µm. In this mode, the light beam with 6w/µm power is launched into the waveguide 1 continuously and all input light beams are applied to A port synchronously. The B and C ports are represented XOR and NOR logical gates, respectively.

In the following, we analyze both these modes and show their simulation results with more details.

2.2.1 NAND gate

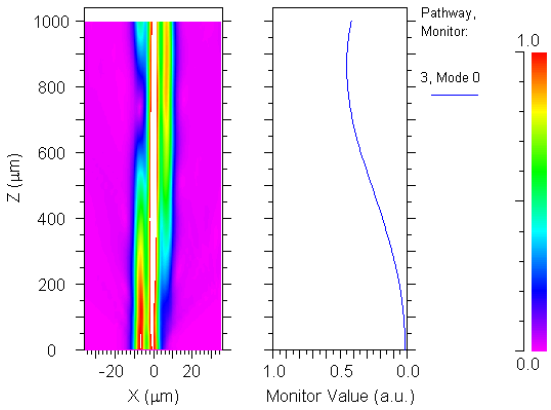
A light beam with 4 w/μm power considered as logical one and the light beam with 4 w/μm power is launched into the waveguide 1 consistently. In first state, when inputs are zero logic, there is no light in A port, due to the same refractive indices of waveguides, the coupling occurs between the waveguides and control light inside the waveguide 1, exits from B port. This state is shown in figure 4.



Input		NAND
0	0	1

Figure 4. Normalized output power (unit: w/μm) in first state, when no lights exists in the input, the output of NAND gate is logical one; and Truth table of the first state.

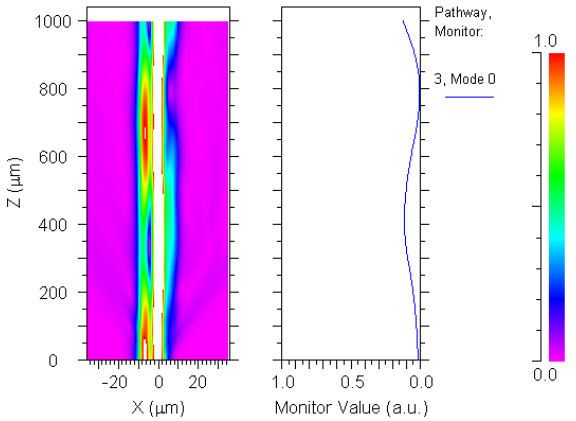
In second state, when only one input is logical one, it means that the beam with 4 W/μm in power launched to the A port. Because of the nonlinear feature of waveguide 2, this control power can increase the refractive index of waveguide 2 and incomplete coupling occurs between the waveguide 2 and 3, therefore a light beam with 4w/μm (logical one) emerges from the B port (Figure 5).



Input		NAND
0	1	1
1	0	1

Figure 5. Normalized output power (unit: w/μm) in second state, when only one input is logical one, the output of NAND gate is logical one; and Truth table of the second state.

In the third state, when both of inputs are logical one, it means that the beam with 8 w/μm in power applied to the A port, according to nonlinear feature of input port, 8 w/μm power can increase the refractive index of this waveguide (waveguide 2) but the coupling between the waveguides 2 and 3 will not occur, so there is no light at the end of B port as shown in figure 6.



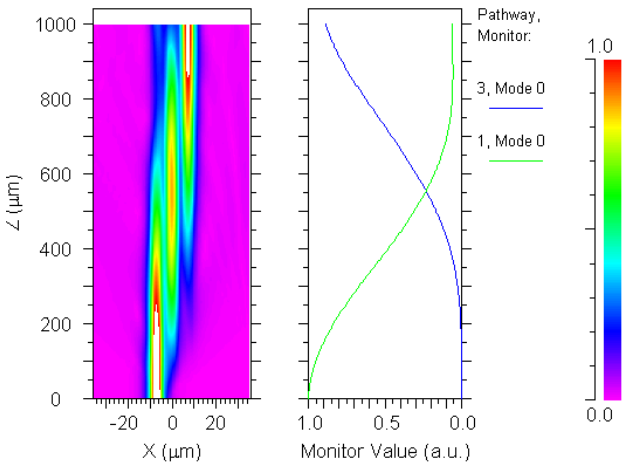
Input		NAND
1	1	0

Figure 6. Normalized output power (unit: w/µm) in third state, when both of inputs are logical one, the output of NAND gate is logical zero; and Truth table of the third state.

In above, the operation of NAND gate by use of nonlinear directional coupler is achieved. In this design, the input light beam with 4 w/µm in power is considered as logical one and the output from the structure is the light beam with 4 w/µm; so the output light beam of this gate can be used as an input light beam of the same gate in the next stage. In other words, this gate has the capability of cascading with other gates. The cascading feature is necessary in the integrated circuits.

2.2.2 NOR/XOR gates

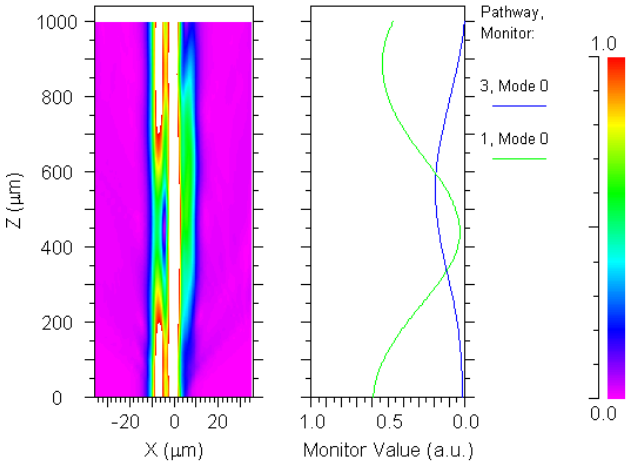
In second mode, a light beam with 6 w/µm in power considered as logical one and the control beam with 6w/µm power is launched into the waveguide 1 continuously. The first state of NOR/XOR gate is similar to the first state of NAND gate. In other words, there is no light in the A port therefore, the coupling will be occurred between three waveguides due to their equal refractive indices and the constant light beam int the waveguide 1, emerges from B port (NOR gate) and there is no light at the C port (XOR gate) as shown in figure 7.



Input		NOR	XOR
0	0	1	0

Figure 7. Normalized output power(unit: W/µm) in first state, when no lights exists in the input, the output of NOR gate is logical one, blue curve, and output of XOR gate is logical zero, green curve; and Truth table of the first state

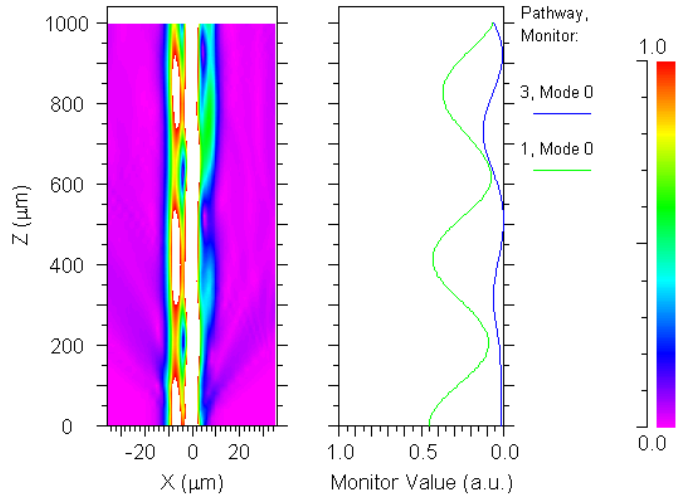
In the second state, only one of the inputs is logical one, it means that the beam with 6 W/μm power is launched to the A port therefore, refractive index of waveguide 2 is increased due to its nonlinear properties. But the coupling between the waveguides 2 and 3 will not occur hence, the light exits from B port and the constant light with 6 w/μm power is remained into the waveguide 1 and exits from C port. Figure 8 shows this state of inputs.



Input		NOR	XOR
0	1	0	1
1	0	0	1

Figure 8. Normalized output power(unit: W/μm) in second state, when only one input is logical one, the output of NOR gate is logical zero, blue curve, and output of XOR gate is logical one, green curve; and Truth table of the second state.

In third state both of inputs are logical one, it means that the beam with 12 w/μm enter to the A port. The refractive index of waveguide 2 increased because of its nonlinear behavior. But this amount of increment does not cause to coupling event between waveguide 2 and 3, so there is no light can exit from the B port. On the other hand, the control light in the waveguide 1, enters to the waveguide 2, therefore there is no light emerges from C port. This event is occurred in the length of 1000 μm. This state is shown in figure 9.



Input		NOR	XOR
1	1	0	0

Figure 9. Normalized output power(unit: W/μm) in third state, when both of inputs are logical one, the output of NOR gate is logical zero, blue curve, and output of XOR gate is logical zero, green curve; and Truth table of the third state.

In above, by use of nonlinear directional couplers, the operation of NOR and XOR gates was obtained. In this design, these gates can be cascaded with other gates in next stage similar to NAND gate.

Finally, the group delays (GD) and Insertion loss (I.L.) of the proposed logical gates have been calculated by these equations:

$$GD(ns) = \frac{L}{c \times \sqrt{1-\left(\frac{c}{2af}\right)^2}} \quad (6)$$

$$I.L.(dB) = 10\log_{10}\left(\frac{P_{out}}{P_{in}}\right) \quad (7)$$

In which, in equation 6, c is the speed of light (29.979 cm/ns), a is the width of waveguides (cm) and L is the length of gates. In equation 7, PoutPin are the output and input power in each waveguide.

The amount of GD and Insertion loss of designed gates are shown in tables 2 and 3.

Table 2. Group delay of the proposed gates

Group delay	NAND	NOR/XOR
Pico-second (Ps)	3.3	3.3
Bit-rate (Giga bit per seconds)	303	303

Table 3. Insertion loss of the proposed gates

Input	Insertion Loss (dB)					
	NAND			NOR/XOR		
	Waveguide 1	Waveguide 2	Waveguide 3	Waveguide 1	Waveguide 2	Waveguide 3
00	-13	-11.2	-0.46	-13	-11.8	-0.54
01,10	-10	-2.2	-3.7	-3.5	-1.9	-
11	-20	-0.7	-10	-13	-1.2	-13

3. Conclusion

The NAND and NOR gates are used in digital circuits design. These gates are called universal gates as any digital function can be implemented by using just NAND or NOR gate. We presented a new structure for all-optical logic NAND, NOR and XOR gates based on nonlinear directional coupler and experimentally demonstrated these schemes by using Rsoft's BeamPROP simulator. One of the advantages of all optical logic gates is high speed of gate operation in comparison with electrical gates. On the other hand, the logical gates are designed with NLDCs are compact and potentially applicable for photonic integrated circuit; also their structure is simpler than other techniques.

4. References

[1] Kun.Yi Lee, Jhe-Min Lin, Yi-Cheng Yang, Yi-Bin Yang, Jia-SingWu, Yu-Tai Huang, Yen-Juei Lin, Kuen-Cherng Lin, Wei-Yu Lee: The Designs of XOR Logic Gates Based on Photonic Crystals. No.245, Academia Rd., Sec. 3, Nangang District, Taipei City 115, Taiwan.

[2] A.P. Kabilan 1, X. Susan Christina 2, P. Elizabeth Caroline3: realization of optical logic gates using photonic crystal. International Conference on Optics and Photonics Chandigarh (2009).

[3] D.Nesset, M.C.Tatham, D.Cotter: High bit rate operation of an all-optical AND gate by using FWM in an SLA with degenerate input signals. Optical Fiber Communication, Optical Society of America, Washington, D.C., (1995).

[4] J. H. Kim, B. C. Kim, Y. T. Byun, Y. M. Jhon, S. Lee, D. H. Woo, and S. H. Kim: All-optical AND gate using cross-gain modulation in semiconductor optical amplifiers. Japanese J. Appl. Physics, 43(2), 608--610 (2004)

[5] H.Soto, C.A.Díaz, J.Topomondzo, D.Erasme, L.Schares, G.Guekos, "All-Optical AND gate implementation using cross polarization modulation in a semiconductor optical amplifier," IEEE Photon. Technol. Lett. 14, 498-500, 2002.

[6] J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane: A Terahertz Optical Asymmetric Demultiplexer (TOAD). IEEE Photonics Technology Letters, 787--790 (1993).

[7] N. S. Patel, K. A. Rauschenbach, and K. L. Hall: 40-Gb/s Demultiplexing Using an Ultrafast Nonlinear Interferometer (UNIT). IEEE Photonics Technology Letters, 8(12), 1695--1697 (1996).

[8] Claudio Porzi, Mircea Guina, Antonella Bogoni, and Luca Pot`ı: All-Optical NAND/NOR Logic Gates Based on Semiconductor Saturable Absorber Etalons. IEEE journal of selected topics in quantum electronics, vol . 14, no. 3 (2008).

[9] Joo-Youp Kim, Jeung-Mo Kang, Tae-Young Kim, and Sang-Kook Han: All-Optical Multiple Logic Gates With XOR, NOR, OR, and NAND Functions Using Parallel SOA-MZI Structures: Theory and Experiment. journal of light wave technology, vol. 24, no. 9 (2006).

[10] Young Jin Jung1, Sunkyu Yu1, Sukmo Koo1, Hyungsuk Yu1, Sanghun Han1, Namkyoo Park1, Jae Hun Kim2, Young Min Jhon2 and Seok Lee2: Reconfigurable all-optical logic AND, NAND, OR, NOR, XOR and XNOR gates implemented by photonic crystal nonlinear cavities. IEEE (2009).

[11] J.Y. Kim, J.M. Kang, T.Y. Kim and S.K. Han: 10 Gbits all-optical composite logic gates with XOR, NOR, OR and NAND functions using SOA-MZI structures. electronics letters, Vol. 42 No. 5 (2006).

[12] Le Trung Thanh: All-optical NAND and AND gates based on 3x3 general interference multimode interference couplers. VNU Journal of Science, Mathematics 108 - Physics 26 (2010).

[13] H.-F. Yau1, H.-Y. Lee2, N.-J. Cheng1: Incoherent all-optical NAND-, NOR-, and XOR-gate using photorefractive fanning effect. Applied Physics B, Lasers and Optics, Springer-Verlag (1999).

[14] G.P.Agrawal: Nonlinear Fiber Optics. Academic Press, New York (1995).

[15] B.E.A. Saleh, M.C. Teich: Fundamentals of photonics. A Wiley-Interscience publication (1991).

[16] Gin´es Lifante: Integrated Photonics Fundamentals. John Wiley & Sons Ltd, The Atrium, Southern Gate, Chichester,West Sussex PO19 8SQ, England (2003).

[17] A. Bananej, S. M. Hamidi, W. Li, C. Li, M. M. Tehranchi: A flexible design for one-dimensional photonic crystals with controllable photonic bandgap width. Optical Materials 30, 1822--1827 (2008).